Introduction

This data sheet details the Embedded-Electrician in-system voltage drop IP Core invented and developed by Isra-Juk Electronics Ltd.

Key features

- Synthesizable, technology independent VHDL IP Core
- Enables in-system, real-time measurement of voltage drop on a power line
- Enables detection of voltage discontinuities on the power line
- Supports various line voltages and line-frequencies
- Helps in early detecting of electrical faults on electrical wiring of a facility
- Enables detecting waste of energy on the of wiring of an electrical facility

Applications

- Electricity monitoring in industrial-internet systems
- Detection of electrical problems by home control, SCADA and industrial internet systems
- IOT feature – enables appliances to detect problems in the electrical power supplied to them
- Enables electricians to detect electrical problems that are not detected by present equipment

General Description

This block monitors the power line and supplies data that enables detection of electrical faults on the power line.

Some of the faults can be immediately detected. Other faults can be detected by comparing readouts from the core with readouts from measurements performed at other points in the electrical system. Additional electrical faults can be detected by tracking the readouts over time.

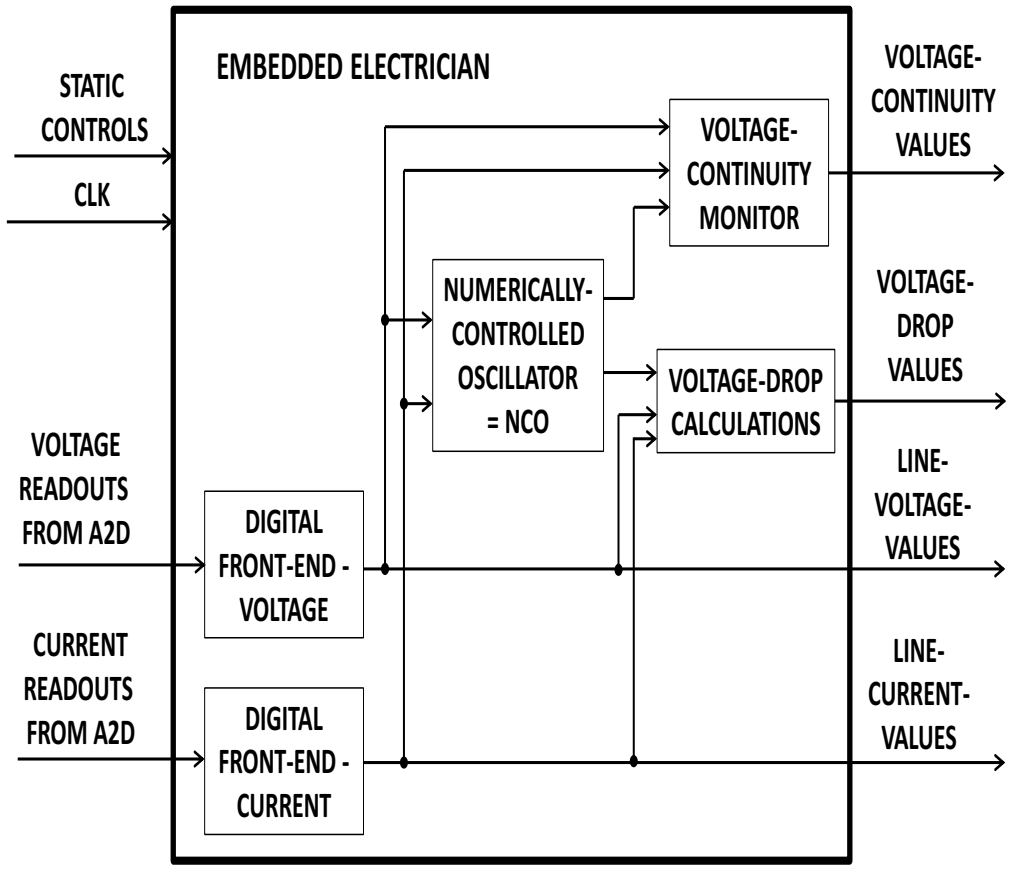
The core provides two primary measurements:

- Percentage of voltage drop on the wiring
- Time that elapsed since voltage discontinuity occurred.

Voltage drop on wiring is computed by integrating the difference between the voltage present when there is current flow on the wiring and the voltage present when there is now current flow over the whole AC cycle.

Time that elapsed since voltage discontinuity occurred is a parameter that enables detection discontinuities on the electrical wiring. Analysis of the readouts of this parameter from several locations in an electrical facility can help in distinguishing between a discontinuity in a common part of the wiring and a discontinuity in a specific branch of the wiring.

Block diagram



Blocks Description

- Digital front-end voltage:
  This block performs the following functions:
  - Line frequency metering
  - Line voltage metering
  - Voltage DC removal
  - Line voltage compensation

- Digital front-end current:
  This block performs the following functions:
  - Current metering – peak voltage
  - Current metering – RMS calculation
  - Current DC removal
  - Line current compensation

- Numerically Controlled Oscillator:
  This block implements an 'NCO' (numerically controlled oscillator) that is locked to the input AC voltage when there is no current consumption by the load. The NCO generates a signal that represents the expected voltage waveform.

- Voltage drop calculations: This block calculates the percentage of the voltage drop on the line. The block integrates the expected voltage value over a complete AC cycle and integrates the difference between the actually measured voltage and the expected voltage, over complete AC cycles. These calculations are done more than 4,000 times per one AC cycle. The block divides the sum of the differences between the expected and actual voltages by the overall expected voltage for each AC cycle. The result of this division is the fraction of the voltage drop on the line.

- Voltage continuity monitor: This block counts the time that elapsed from the power-up of the system and the time that elapsed since a discontinuity occurred on the AC line. When no discontinuity occurred since the module was powered up, these two values will be the same. In case a discontinuity occurs on the line, there will be difference between these values. Analysis of readouts from several monitoring units can help in identifying and locating the cause of the electrical discontinuity that occurred.

A2D interface - parallel

Pinout Description

The following table details the pinout of the present core. Adoptions can be made upon requests from customers.

Port name	Width	direction	Active state	Description
General:				
sys_rst	1	Input	high	active-high asynchronous reset
sys_clk	1	Input	Rising -edge	12.5 MHz clock
system timing				
en_1_sec	1	Input	high	1-clock-cycle pulse, used for frequency voltage metering and control-interface update
cycle_start_ indication	1	Output	high	1-clock-cycle pulse, indicates start of an AC cycle, used for debug
cycle_ boundaries_ data_valid	1	Output	high	indicates that the cycle_boundaries_data is valid, used for debug
Static controls: System-level controls				
freq_range	2	Input	data	00 = 50 Hz, 01 = 60 Hz, 10 = 400 Hz, 11 = 400 Hz.
input_is_dc	1	Input	data	'1' = measured voltage is DC, '0' = the measured voltage is AC
voltage_range	2	Input	data	00 = 100V, 01 = 110V, 10 = 220V, 11 = 230V
voltage_a2d_f s_voltage	10	Input	data	positive line-voltage that is represented by the +full-scale value of the

Port name	Width	direction	Active state	Description
				voltage-A2D
Static controls: NCO lock controls				
nco_lock_ enable_switch	1	Input	high	1 enables locking of the NCO to input AC-sine, 0 sets the NCO free run
nco_phase_in _ctr_offset	18	Input	data	Initial offset for the phase-in counter. Should be set to 0x1.
cycle_length_ remainder_ increment	7	Input	data	Control NCO tracking of multiple AC cycles. Set to 0.
Static controls: NCO calibration controls				
nco_cal_use_ cal_result	1	Input	data	1 - use NCO-calibration results, 0 - use default values
nco_cal_start_ pulse	1	Input	high	1 - forces NCO calibration start, 0 – no effect on calibration start
nco_phase_to _mult_initial_ offset	8	Input	data	Initial NCO phase value. Should be set to 0x27.
nco_cal_start_ offset_value	8	Input	data	Should be set to 0x20
nco_cal_end_ offset_value	8	Input	data	Should be set to 0x40
voltage readouts from A2D				
voltage_ readout_mult_ factor	18	Input	data	Value in which the readout from the voltage A/D should be multiplied
voltage_ readout_div_ factor	18	Input	data	Value in which the readout from the voltage A/D should be divided
volt_a2d_core _data_input	14	Input	data	raw data from voltage A/D
volt_a2d_core	1	Input	high	Indicates when the data

Port name	Width	direction	Active state	Description
_data_strobe				from the voltage-A/D is valid
current readouts from A2D				
crnt_a2d_raw_data	14	Input	data	raw data from current A/D
crnt_a2d_raw_data_strobe	1	Input	high	Indicates when the data from the current-A/D is valid
continuity-detection control				
delta_value_for_treating_as_spike	10	Input	data	Minimum difference between measured and expected voltage – that will be treated as a spike
min_level_in_voltage_for_checking	10	Input	data	Minimum voltage level (positive or negative) to begin checking for spikes
outputs to the voltage-display logic				
dc_removal_correction_value	14	Output	data	DC component of the line-voltage
peak_line_voltage	14	Output	data	Peak value on the measured voltage
voltage_sign	1	Output	data	0 - measured line voltage is positive, 1 - measured line voltage is negative
voltage_valid	1	Output	data	1 - voltage is in the allowed range, 0 - voltage is outside the allowed range
frequency measurement				
measured_freq	16	Output	data	The frequency of the measured voltage – in Hz
freq_valid	1	Output	data	1 - measured frequency is in the allowed range 0 - measured frequency is

Port name	Width	direction	Active state	Description
				outside the allowed range
voltage-drop calculations				
voltage_drop_ fraction	10	Output	data	Binary fraction of voltage drop on the wiring
continuity-counting				
discontinuity_ error_occured	1	Output	data	a positive pulse indicates that a discontinuity-error occurred on the measured voltage
seconds_ overflow	1	Output	high	'1' indicates that an overflow occurred on the seconds-from-discontinuity counter
seconds_from _power_up_ counter	16	Output	data	counts the seconds that elapsed since the system was powered-up
seconds_from _discontinuity _ counter	16	Output	data	counts the seconds that elapsed since voltage discontinuity occurred
current-related values				
value_of_zero _current	14	Output	data	Offset-value of the current-sensor – in mA Signed value
rms_data_out	12	Output	data	current-level in mA
load_active	1	Output	data	1 indicates that the load is active, 0 indicates load is not active load-active is determined by current-level
debug outputs				
cycle_1_4_way _ind	1	Output	data	indicates the point of a fourth of a cycle in the AC voltage
cycle_ envelope	1	Output	data	MSB of the radian-counter of the NCO

FPGA Resources

This VHDL core is technology independent. In order to estimate core size - synthesis results are provided for the Xilinx® Spartan3 FPGA devices. Synthesis results for other FPGAs and technologies can be provided on request.

FPGA Resource	Xilinx Spartan-3	Xilinx Artix 7	Altera Cyclone
Tool Used to compile	ISE 14.7	Vivado 2015.3	Quartus 15.1
Look-up Tables	2,845	2,541	
Flip-Flops	3,122	2,124	
Block RAM	4 * RAMB16	1 * RAMB18	
Multipliers	5 * mult18x18	5 DSP blocks	

Simulation

A test bench is supplied with the VHDL code using Xilinx Spartan-3 FPGA.

Testing

The design was tested in a lab setup of 220V @ 50 Hz.

Legal Notice

Parts of this design are covered by USA, Canada, Europe & Israel granted patents.

Other parts are patent pending.

All trade-marks mentioned belong to their owners.

Disclaimer

Isra-Juk assumes no liability to the usage of this design.

Availability

This design is available as a synthesizable VHDL code.

The design can be supplied as an electrical module upon request.

Additional information, including application-notes, can be obtained from Isra-Juk Electronics.

About Isra-Juk Electronics

Isra-Juk Electronics Ltd is a privately-held Israeli company that

- Develops electricity-monitoring technologies.
- Acts as a d\sub-contractor for electronic designs.

Contact Information

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Revision History

Revision	Date	Change Description
1.0	18-Nov-2015	Initial revision